

REMARKS

Claims 1-30 are pending in this application. In the last office action, the IDS was found to be not in compliance with 37 C.F.R. § 1.98(a). In addition, claims 1-3, 15-19 and 25-30 were rejected under 35 U.S.C. § 112, 2nd paragraph, as being indefinite. Claims 1-15 and 20-30 were rejected under 35 U.S.C. § 102 as being anticipated by Winters et al (U.S. Patent No. 6,292,818). Finally, claims 16-19 were objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. Applicant gratefully acknowledges this indication of allowability.

This Response amends claims 1-4, 10, 12-13, 16, 20, 23, 25, and 27, cancels claims 15 and 22, and adds new claim 31, to better define the invention without prejudice or disclaimer of the subject matter of the claims as initially filed for possible prosecution in a subsequent continuation application. In addition, although Applicant does not necessarily agree with the Examiner's conclusion that claims are unpatentable, the above-stated amendments have been made to expedite prosecution of this application.

1. The Fururki reference on the IDS is enclosed herein and should now be considered

The last office action noted that the IDS filed 11/18/02 was not filed with a copy of a foreign patent document, JP 5-259893 by Furuki, although the IDS was filed with an English language abstract of this document. At the time of filing this IDS, Applicant did not have a copy of this foreign patent document. A copy of JP 5-259893, along with another copy of the English language abstract, is being filed herein with the present Response to Office Action. Applicant respectfully requests that this document be considered by the Examiner.

2. The rejections under § 112, 2nd paragraph should be withdrawn

The last office action noted certain minor informalities in claims 1 and 2. These claims have been amended to more clearly define the invention claimed. Claim 15, which was rejected under § 112, 2nd paragraph, has been cancelled. As to claim 25,

Applicant directs the Examiner's attention to FIG. 4 of the present application and submits that claim 25 accurately describes the circuit shown in FIG. 4.

Thus, Applicant respectfully requests that the Examiner withdraw the rejections under 112, second paragraph, of these claims and of claims 3, 16-19, and 26-30, which depend upon one of claims 1, 2, 15 or 25.

3. Claims 1-9 are allowable over Winters and the art of record

Applicant submits that claims 1-9 are patentable over Winters and the art of record. As amended, independent claim 1 recites "a symmetric differential domino carry generate circuit having true inputs and compliment inputs which both have a load, wherein the load for the true inputs is equal to the load for the compliment inputs" (emphasis added).

As amended, independent claim 4 recites a differential domino carry generate circuit that has "a true carry generate output and a compliment carry generate output which both have an output drive strength, and wherein the output drive strength for said true output is the same as the output drive strength for said compliment output" (emphasis added).

Applicant submits that Winters does not disclose or suggest any characteristics of:(1) the load for any inputs, or (2) the output drive strength for any outputs. Moreover, Winters does not inherently disclose the recited limitations; inherency is only proper where the reference necessarily discloses the recited limitations. See MPEP § 2112 ("The mere fact that a certain thing may result from a given set of circumstances is not sufficient.") (quoting *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999)). Because Winters does not disclose the recited limitations, the rejection of claims 1 and 4 as anticipated by Winters is improper.

Applicant also submits that there is no evidence to modify the art of record to obtain the processor recited in claims 1 and 4. Applicant notes that, to support an obviousness rejection, an Examiner must "point to some concrete evidence in the record" of a motivation to combine or modify the references as asserted. See, e.g., *In re Zurko*, 258 F.3d 1379, 1368 (Fed. Cir. 2001).

For at least these reasons, claims 1 and 4 are believed to be patentable. Claims 2-3 and 5-9 depend from claim 1 or 4 and are patentable for at least the same reason as these claims.

4. Claims 10-14 and 16-19 are allowable over Winters and the art of record

Applicant submits that claims 10-14 and 16-19 are patentable over Winters and the art of record. As amended, independent claim 10 recites an apparatus that includes a first evaluation block that comprises “a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor.” (emphasis added).

Applicant submits that Winters does not disclose or suggest a first evaluation block that comprises “a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor” as recited in claim 10.

In rejecting claim 10, the last Office Action relied upon FIG. 6 of Winters. Applicant submits that the circuit shown in FIG. 6 of Winter does not teach or suggest an evaluation block with a transistor that has a drain that is connected to the source of two other transistors in the evaluation block, as is the case for the “fourth transistor” recited in Applicant’s claim 10.

For at least these reasons, claim 10 is believed to be patentable. Claims 11-14 and 16-19 depend from claim 10 and are patentable for at least the same reason as that claim.

5. Claims 20-21 and 23-24 are allowable over Winters and the art of record

Applicant submits that claims 20-21 and 23-24 are patentable over Winters and the art of record. As amended, independent claim 20 recites and apparatus that

comprises “a first evaluation block connected to the current input, the true sum output, and the compliment sum output, . . . wherein the first transistor has a drain connected to the compliment sum output, the second transistor has a drain connected to the source of the first transistor and a source connected to the drain of the fifth transistor, the third transistor has a drain connected to the true sum output, the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor, and the fifth transistor has a source connected to the current input.” An example of such a circuit is shown in FIG. 4 of the present application.

Applicant submits that Winters does not disclose or suggest “a first evaluation block connected to the current input, the true sum output, and the compliment sum output, . . . wherein the first transistor has a drain connected to the compliment sum output, the second transistor has a drain connected to the source of the first transistor and a source connected to the drain of the fifth transistor, the third transistor has a drain connected to the true sum output, the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor, and the fifth transistor has a source connected to the current input” as recited in claim 20.

In rejecting claim 10, the last Office Action relied upon FIG. 6 of Winters. However, Winters does not teach or suggest “a first evaluation block connected to the current input, the true sum output, and the compliment sum output.” In addition, Winters does not teach or suggest a “fifth transistor” that has a source connected to the current input, a “second transistor” that has a source connected to the drain of the fifth transistor, a “fourth transistor” has a source connected to the drain of the fifth transistor. Nor does Winters teach or suggest a “third transistor” that has a drain connected to the “true sum output.”

For at least these reasons, claim 20 is believed to be patentable. Claims 21 and 23-24 depend from claim 20 and are patentable for at least the same reason as that claim.

6. Claims 25-30 are allowable over Winters and the art of record

Applicant submits that claims 25-30 are patentable over Winters and the art of record. As amended, independent claim 25 recites a method that includes processing compliment input values at a second evaluation block to provide a carry generate value “by selecting one of a plurality of stacks of transistors in the second evaluation block, wherein each of said stacks of transistors connects a current input to the first output” and processing true input values to provide the compliment of a carry generate value “by selecting one of a plurality of stacks of transistors in the first evaluation block, wherein each of said stacks of transistors connects said current input to the second output” (emphasis added).

Applicant submits that Winters does not disclose or suggest a method that includes processing compliment input values at a second evaluation block to provide a carry generate value, or processing true input values at a first evaluation block to provide the compliment of a carry generate value, as recited in claim 25.

In rejecting claim 25, the last Office Action relied upon FIG. 6 of Winters. Applicant submits that the circuit shown in FIG. 6 of Winters does not teach or suggest a second evaluation block to provide a carry generate value or processing true input values at a first evaluation block to provide the compliment of a carry generate value, as recited in Applicant’s claim 25. The outputs of the three transistors in FIG. 6 that have inputs C1L and VDD, C1H and VDD, and B1L are used to generate both SNUM and SUM. Thus, because they are used to generate both values, neither is part of a “second evaluation block to provide a carry generate value” or a “first evaluation block to provide the compliment of a carry generate value.” Similarly, the remaining transistors in the circuit are neither part of a first evaluation block or second evaluation block as recited in claim 25 because these transistors cannot provide a carry generate value or a compliment carry generate value without the aforementioned three transistors in FIG. 6 that have inputs C1L and VDD, C1H and VDD, and B1L.

For at least these reasons, claim 25 is believed to be patentable. Claims 26-30 depend from claim 25 and are patentable for at least the same reason as that claim, and for any additional limitations in the dependent claims. An example of such additional limitations is found in claim 31, that recites that “the first evaluation block has three stacks of transistors” and that “the second evaluation block has three stacks of

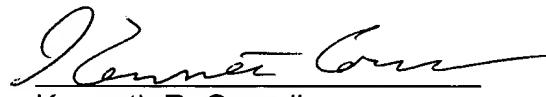
transistors." Applicant submits that neither Winters or any other prior art show this additional limitation of claim 31.

7. Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Kenyon & Kenyon Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application.

Respectfully submitted,

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